JEATSA JOURNAL
JOURNAL OF ENGINEERING ADVANCES AND TECHNOLOGIES FOR SUSTAINABLE APPLICATIONS
Volume 1, Issue 1 (January, 2025)
Print ISSN: 3062-5629 Online ISSN: 3062-5637
Open Access
https://jeats.journals.ekb.eg/

High-Speed High-Swing Charge-Steering Latches

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doi: 10.21608/jeatsa.2025.427800
Received 29-8-2024
Revised 10-10-2024
Accepted: 1-11-2024
Published: Jan-2025

Print ISSN: 3062-5629
Online ISSN: 3062-5637

Abstract- This paper introduces two novel charge-steering (CS) latches that can achieve a high output swing by accelerating the operation of the tail capacitor. These latches are particularly well-suited for use in hybrid circuits, such as demultiplexers (DEMUXs) and clock and data recovery (CDR) systems, as well as in mixed-mode circuits like analog-to-digital converters (ADCs). The proposed latches address the increasing demand for power-efficient solutions in high-speed transceivers, where balancing performance and energy consumption is critical. Implemented using 40-nm CMOS technology, the latches operate at data rates of 28 Gb/s while consuming only 290 µW and 304 µW from a 1V supply. They achieve differential output swings of 941 mVpp and 1.22 Vpp. This represents a significant improvement in output swing. By incorporating NMOS capacitors in the tail, the latches demonstrate an increase in output swing of up to 50% compared to previous designs, with only a small increase in power consumption. Simulation results confirm the high-speed performance and power efficiency of the design, making it highly suitable for next-generation communication systems.

Keywords- *Charge Steering, Clock and Data Recovery, Analog Digital Converter, Demultiplexer*.

I. INTRODUCTION

The demand for low power consumption circuit designs continues to grow, driven by the increasing need for high-speed data transceivers in modern communication systems and computing applications. As operational frequencies rise, the traditional power-speed trade-off becomes increasingly nonlinear, making maintaining high performance and energy efficiency challenging. Recent advancements aim to achieve a power efficiency benchmark of approximately 1 mW/Gb/s. However, as data rates exceed 25 Gb/s, maintaining this efficiency becomes difficult due to conventional designs' quadratic relationship between frequency and power consumption. Charge-Steering (CS)-based circuits have demonstrated significantly lower power consumption compared to earlier current-mode logic, achieving a reduction by a factor of 4.4, with power efficiencies as low as 0.2 mW/Gb/s at data rates ranging from 25 to 40 Gb/s, which present an attractive solution for high-speed applications [1].

This paper introduces two new CS latch topologies with high output swing and enhanced speed capabilities. The proposed latches demonstrate potential for achieving data rates exceeding 28 Gb/s, making them ideal for implementation in hybrid circuits such as demultiplexers (DEMUXs) and clock and data recovery (CDR) circuits, as well as mixed-mode systems like analog-to-digital converters (ADCs).

In Section II, we provide background information on CS latches. In Section III, we introduce the new CS latches for the applications that require high output swing. In Section IV, we evaluate the effectiveness of the new latches. Finally, in Section V, we present our conclusions.

II. BACKGROUND

The basic CS latch shown in Fig. (1), introduced in [1], operates in two modes. In the first mode, when the clock signal (CK) is low, the latch gets in the reset state. The tail capacitor (C_T) is discharged to the ground, while load capacitors (C_{DS}) are charged to V_{DD}, and the differential pair is turned off. In this state, all components are prepared for charge steering. In the second mode, when CK is high, the latch gets in the evaluation state. The C_T connects to the differential pair, steering current from C_{DS} until the voltage on C_T (V_{C_T}) drops below the higher input level by one threshold, at this point, the input's differential voltage is amplified. The peak of V_{C_T} determines the evaluation charge, defining the output swing in conjunction with the values of C_{DS}. These modes alternate with each clock cycle.

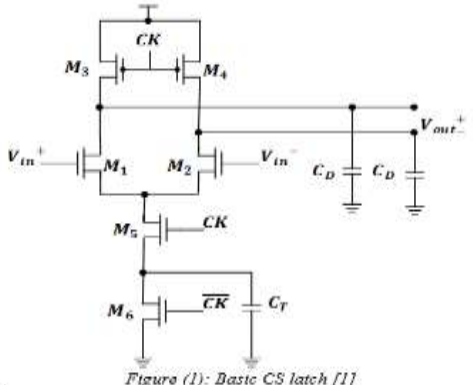

Figure (1): Basic CS latch [1]

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In [10], shown in Fig. (2), a speed-enhancing technique is introduced where the tail capacitor is charged reversely during the reset mode, rather than discharging to ground, allowing it to share charge during the switch from the reset mode to the evaluation mode. This reduces the source voltages of the differential pair, increasing both the output swing and the operating frequency. The tail capacitor is implemented as a NMOS capacitor, which further reduces the differential pair's source voltages compared to a metal capacitor.

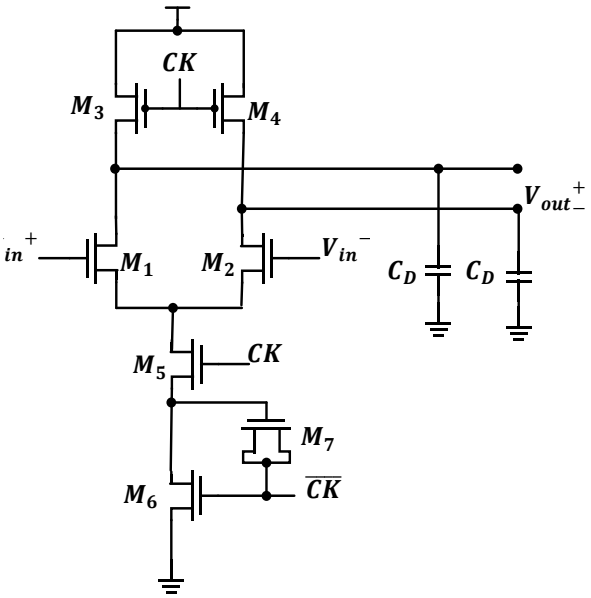

Figure (2): Speeding up CS latch [10]

When cascading the previously mentioned latches, the supply voltage provides the appropriate common-mode level. However, if the gate voltages of the differential pair remain at V_{DD} during charge steering, the drain voltages will drop to $V_{DD} - V_{TH}$, pushing the differential pair into the triode region, resulting in the limited differential swing at the output.

To mitigate this, a cross-coupled (CC) PMOS pair is incorporated on the output nodes, as shown in Fig. (3) [4]. While this restores the high-level output, it introduces a delay that is constrained at high frequencies.

In [11], shown in Fig. 4, the authors present a Non-Return-to-Zero (NRZ) latch by adding a transmission gate (TG) between the basic latch and the CC pair. During the evaluation mode, the TG is on, and the CC pair latches the output. During the reset mode, CC pair stores previous output value.

The described latches [1] [4] [10-11] are very fast and consume low-power, but have limited output swings, making them suitable for use at the front end of a transceiver [7].

For improved performance, two cascode devices, (M_9 and M_{10}), are added, as shown in Fig. (5). These devices isolate the differential pair's drains from the large output node capacitance, increasing the gain from the input voltage to the voltages at the drains. The amplified signal is then transferred to the output via one of the cascode devices, while the other remains off. Further enhancement is achieved by adding another cross-coupled pair, (M_{11} and M_{12},) which increases the voltage gain as the differential pair's drain voltages drop from V_{DD} [5].

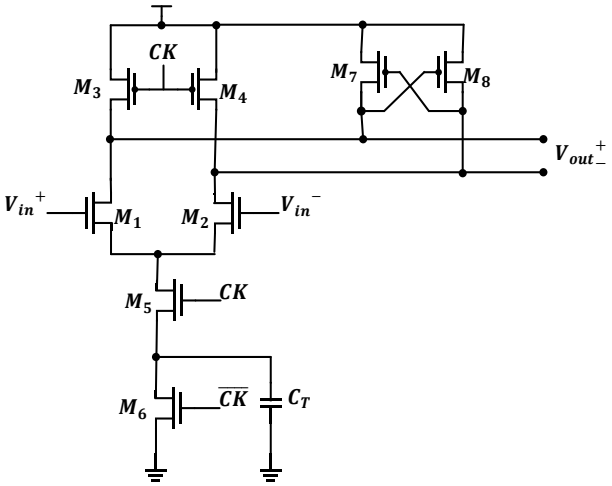

Figure (3): CS latch with a CC PMOS pair [4]

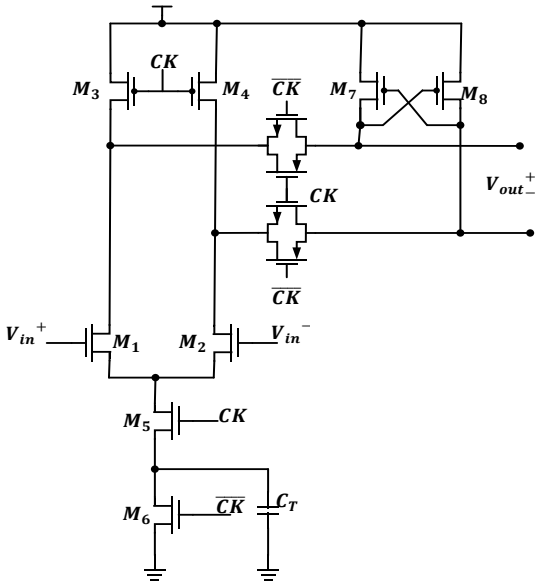

Figure (4): NRZ CS latch [11]

In [7], shown in Figs. (6) and (7), a switch (M_{17}) is added to the CC pair (M_7 and M_8) to reduce power consumption during reset mode.

[7] also eliminates the secondary tail capacitor (C_{ST}), with the CC pair (M_{11} and M_{12}) being pulled to

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ground via (M_{15}), as shown in Fig. (7). This raises the drain voltages of the differential pair, resulting in a greater output swing and reduced power consumption. At high data rates, eliminating the C_{ST} is beneficial as it may not have sufficient time to fully charge, with parasitic capacitances effectively handling regeneration.

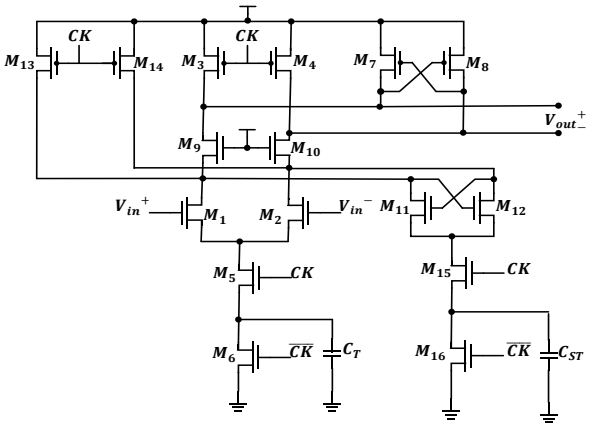

Figure (5): CS latch with a cascode pair [5]

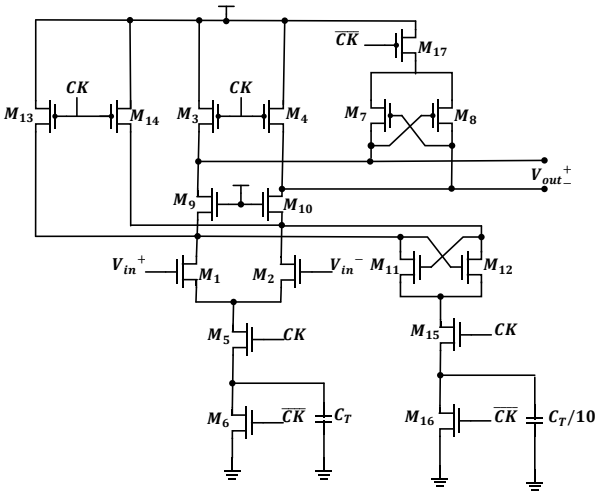

Figure (6): Conventional high-swing CS latch [7]

The latches described in [5] and [7] have high output swings, making them suitable for use at the back end of the transceiver. However, they are unable to operate as quickly as the earlier latches and exhibit significantly higher power consumption.

III. THE PROPOSED CHARGE-STEERING LATCHES

In CS circuits, the load capacitance corresponds to the capacitance at the output and the input of the next stage, and at the output nodes there are no dedicated capacitors. Conversely, the tail capacitors (C_{Ts}) determine the required output swing, with the charge drawn from V_{DD} scaling with C_{Ts} . Consequently, power consumption rises in a linear manner with C_{Ts} up to 10 fF. While increasing the C_{Ts} can compensate for the output swing, it is not recommended, as

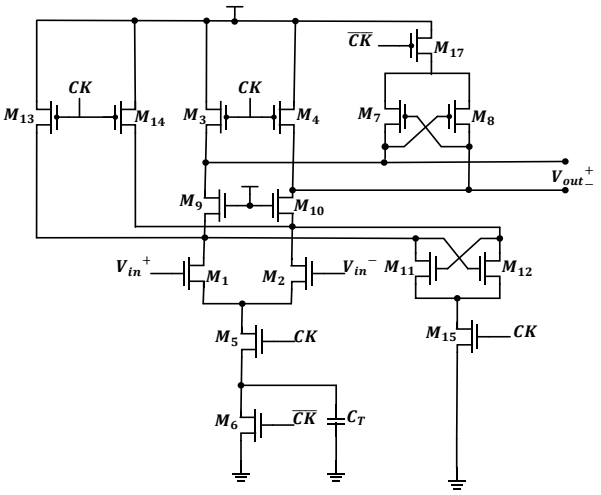

Figure (7): Conventional high-swing CS latch without the secondary tail capacitor [7]

the $\Delta V_{C_{Ts}}$ becomes more susceptible to PVT (Process, Voltage, Temperature) variations [1].

There are two ways to implement these capacitors: 1) metal-oxide-metal (MOM) capacitors and 2) metal-oxide-semiconductor (MOS) capacitors. MOM capacitors are typically preferred due to their high linearity, although they are very sensitive to process variations. In contrast, MOS capacitors show relatively less sensitivity to variations [13].

Reversely charged NMOS tail capacitors are applied to two high-swing latches: one with the NMOS C_{ST} and one without, as shown in Figs. (8) and (9).

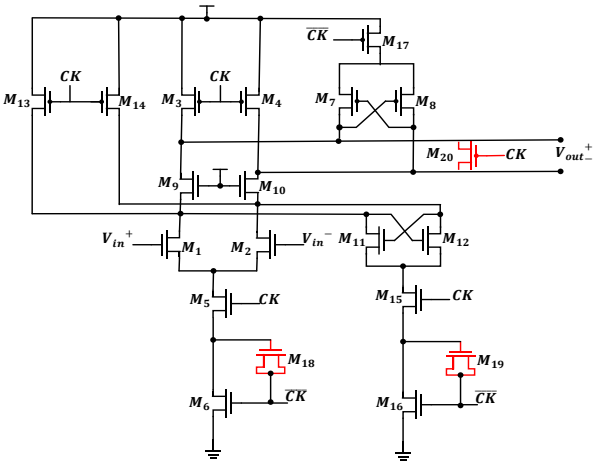

Figure (8): The proposed high-swing CS latch with secondary tail capacitor

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The overlap capacitors between the gate-source and gate-drain enhance operational speed, whereas the gate-bulk capacitor functions as the tail capacitor. The capacitance of the NMOS capacitor is given by:

$$C_{gate} = \frac{\epsilon_{ox} WL}{t_{ox}} \quad (1)$$

where W is the width of the NMOS channel, L is the length of the NMOS channel, ϵ_{ox} is the oxide layer permittivity, and t_{ox} is the oxide layer thickness.

The parasitic capacitors of the source-bulk and drain-bulk contribute as parasitics on the $\overline{CK}$ net. This configuration results in lower source voltages at the differential pair at the starting of the evaluation phase, thus improving the output swing. Additionally, the maximum operating frequencies of these new latches are higher than those of conventional high-swing current-steering (CS) latches.

M_3 and M_4 are the reset switches that during the reset mode precharge the output nodes. To guarantee that the output node stabilizes to V_{DD} within half a clock cycle, these switches must be sufficiently wide; failing to do so may lead to inter-symbol interference (ISI) in the latch [1].

Small PMOS switches have been added between the output nodes of the CS latches to reduce hysteresis, thereby preventing charge waste and allowing for a reduction in the size of the reset switches.

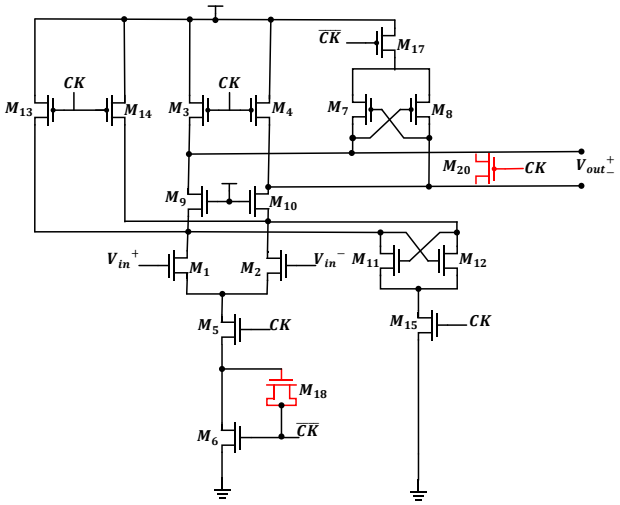

Figure (9): The proposed high-swing CS latch without secondary tail capacitor

IV. SIMULATION

The latches were simulated and compared with previous works under identical conditions using TSMC's 40-nm CMOS technology, characterized by a 1-V power supply. The input data rate was swept from 1 Gb/s to 56 Gb/s, featuring a 100 mVpp differential input swing using Non-Return-to-Zero (NRZ) encoding and an 850 mV common-mode level. All latches were simulated with identical tail capacitors. The values of MOM C_{Ts} in previous works were calculated using Eq. 1. To account for the worst-case scenario, a sinusoidal half-rate clock with an amplitude of 1 V was used for these simulations. The device sizes for all latches are provided in Table (1), with all lengths set to the process minimum of 40 nm, except for the secondary tail NMOS capacitor, whose length is listed in Table (1). These sizes were determined through sweeping simulations to achieve the optimal dimensions that maximize output swing, while considering the design's constraints.

Table (1): CS latches component values

Component	The Opt. Size
$W_{1,2}$	1.4 µm
$W_{3,4}$	600 nm
W_5	9.9 µm
W_6	2.3 µm
$W_{7,8}$	120 nm
W_{17}	1.4 µm
$W_{9,10}$	1.7 µm
$W_{11,12}$	5.6 µm
W_{15}	10.9 µm
$W_{13,14}$	15.3 µm
W_{20}	120 nm
W_{18}	26 µm
W_{16}	30.5 µm
W_{19}	59.6 µm
L_{19}	600 nm
W_{tg}	1 µm
C_T	17 fF
C_{Ts}	571 fF

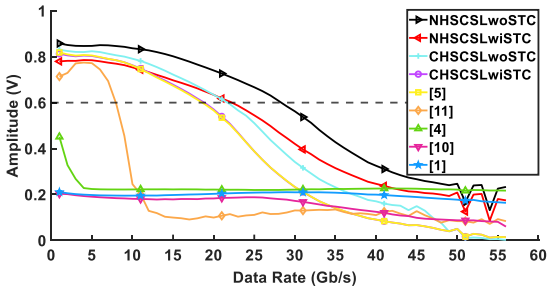

Figure (10): The output swing of CS latches

Fig. (10) shows the output swing versus the operating data rate of the new high-swing CS latch without (NHSCSLwoSTC), the new high-swing CS latch with (CHSCSLwoSTC) (NHSCSLwiSTC), and previous latches, and the conventional high-swing CS latch with

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(CHSCSLwiSTC). The NHSCSLwoSTC provides an output swing 50% higher than the CHSCSLwoSTC at the same operating data rate of 28 Gb/s, while consuming only 4% more power, as shown in Fig. (11).

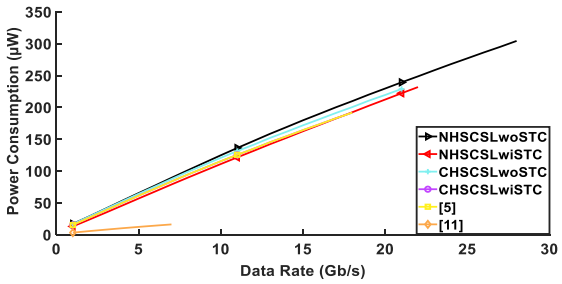

Figure (11): The power consumption of CS latches

Fig. (11) shows the power consumption versus the operating data rate of the latches, which can achieve output swings of 600 mVp.

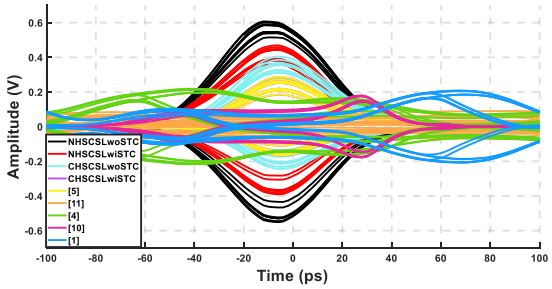

Figure (12): Eye diagram of the output signals of CS latches at 28 Gb/s

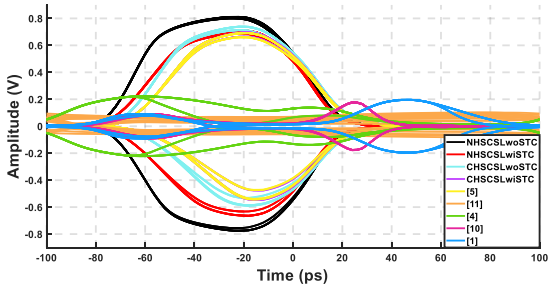

Figure (13): Eye diagram of the output signals of CS latches at 14 Gb/s

Figs. (12) and (13) show the eye diagrams of the output signals of the CS latches at 28 Gb/s and 14 Gb/s, respectively.

The transient waveform of the new CS latches at 28Gb/s can be seen in Fig. (14).

Table (2) provides a comparison with previous works, along the definition of a new Figure of Merit (FoM) as follows:

$$FoM(pJ/b/mV) = \frac{Power\ Consumption}{\frac{Data\ Rate}{Output\ Swing}} \quad (2)$$

While the FoM of the conventional CS latches is better than the proposed ones, using the conventional latches at 28 Gb/s is impossible if a 1.2 Vpp differential swing is needed.

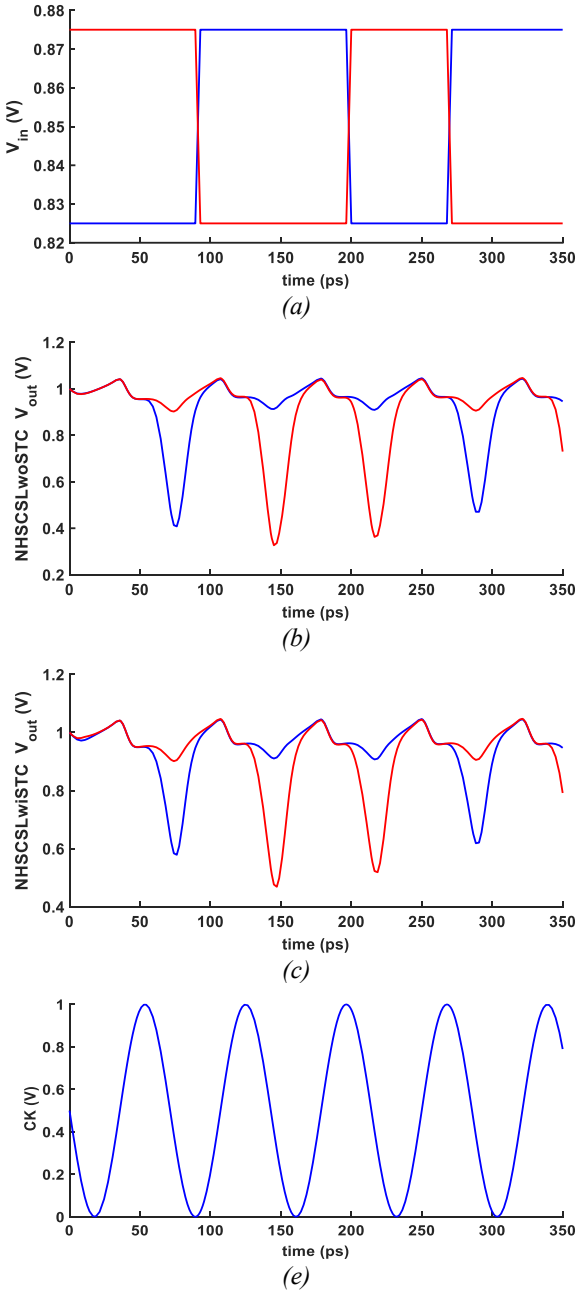

Figure (14): Simulated waveform of new CS latches at 28 Gb/s. (a) the input signal, (b) the proposed high-swing CS latch without secondary tail capacitor output signal, (c) the

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proposed high-swing CS latch with the secondary tail capacitor output signal, and (e) the clock signal

Table (2): Performance summary

References	[1]	[4]	[5]	[7, 8]		[10]	[11]	This Work	
				Conventional High-Swing CS Latch	Conventional High-Swing CS Latch without Secondary Cap			New High-Swing CS Latch	New High-Swing CS Latch without Secondary Cap
Technology (nm CMOS)	65	45	45	28		65	130	40	
Data Rate (Gb/s)	2	12.5	20	28		10	2.4	28	
Supply (V)	1	1	1	1		1	0.6	1	
Clocking	Full rate	Half rate	Half rate	Full rate		Half rate	Full rate	Half rate	
Swing (V)	400m	500m	550m	189m	218m	632m	2.2	470.76m	607.64m
Total Power (μW)	23	-	-	775	638	107.1	10	290	304
FoM (pJ/b/mV)	4.6	-	-	5.23	4.97	6.77	9.17	4.88	6.60

V. CONCLUSION

In this paper, we provide insights into CS latches and propose two new latch designs for high-speed transceivers. We demonstrate that using NMOS capacitors in the tail improves the output swing by up to 50% at high data rates, with only a 4% increase in power consumption compared to previous works under the same conditions. These results were validated through circuit-level simulations in 40-nm CMOS technology.

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